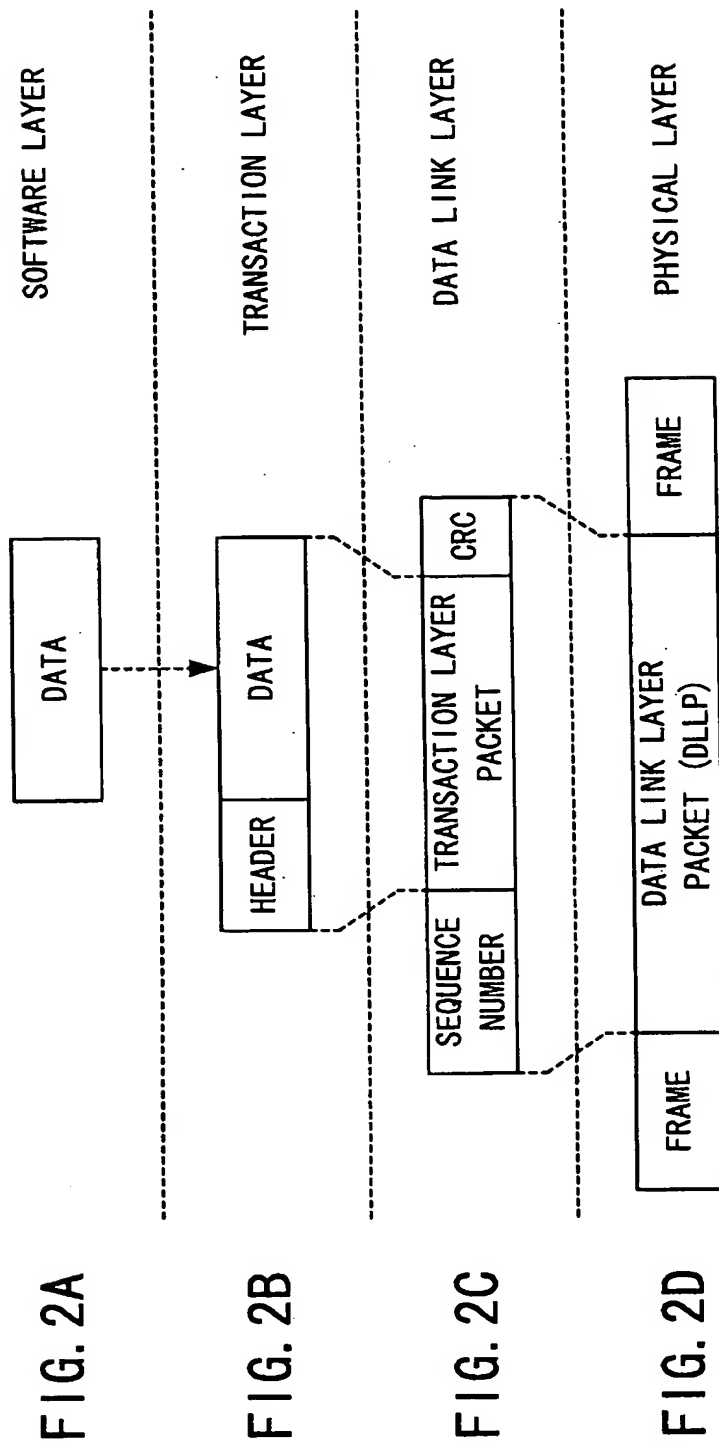


FIG. 1

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**FIG. 3**

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The diagram illustrates a system architecture divided into two main sections: the **INTERNAL CIRCUIT SECTION** and the **40: INTERFACE CIRCUIT SECTION**.

**INTERNAL CIRCUIT SECTION:**

- Contains a **PROCESSOR** (13) and a **MAIN MEMORY UNIT** (14).
- These are connected to a **PROCESSOR** (15) and a **MAIN MEMORY UNIT** (16).
- A **SYNCHRONIZATION BUFFER** (50) is connected to the processor and memory units.
- A **TRANSACTION LAYER** (47) is connected to the synchronization buffer.
- A **COMMUNICATION ERROR PROCESSING SECTION** (46) is connected to the transaction layer.
- A **DATA LINK LAYER (RX)** (44) is connected to the communication error processing section.
- A **DATA LINK LAYER (TX)** (45) is connected to the communication error processing section.

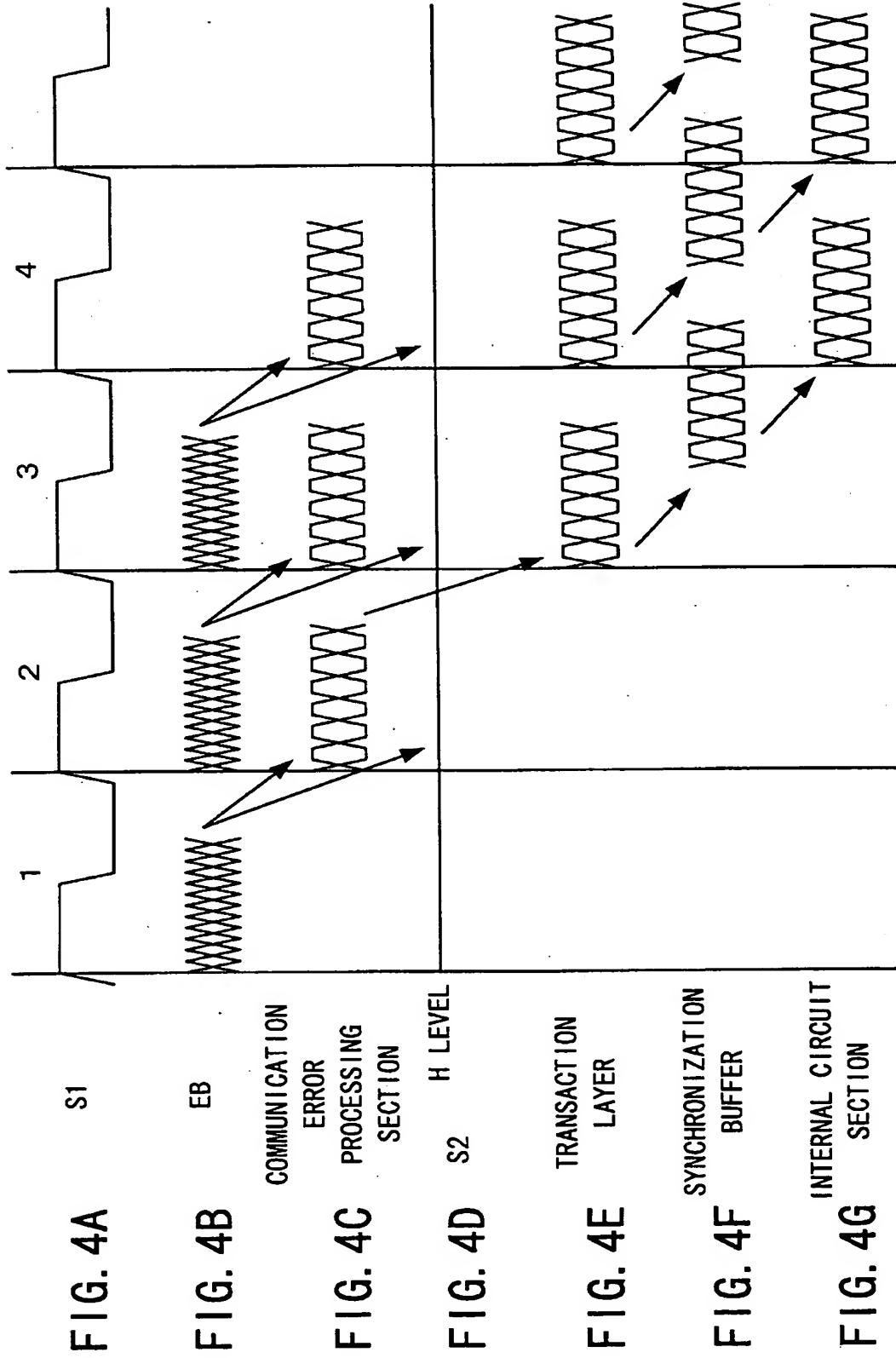
**40: INTERFACE CIRCUIT SECTION:**

- Contains a **DATA LINK LAYER (RX)** (44) and a **DATA LINK LAYER (TX)** (45).
- Each data link layer is connected to a **PHYSICAL LAYER** (43-1, 43-2, ..., 43-n).
- Each physical layer is connected to an **EB** (Error Block).
- The EBs are connected to a **DATA LINK/PHYSICAL LAYER**.

**Other Components:**

- A **MEMORY BRIDGE** (26) is connected to the internal circuit section and the interface circuit section.
- A **FREQUENCY DIVIDER** (31) is connected to the memory bridge and the internal circuit section.
- A **CLK** (Clock) signal is provided to the memory bridge and the internal circuit section.
- A **I/O SYSTEM** (12) is connected to the interface circuit section.

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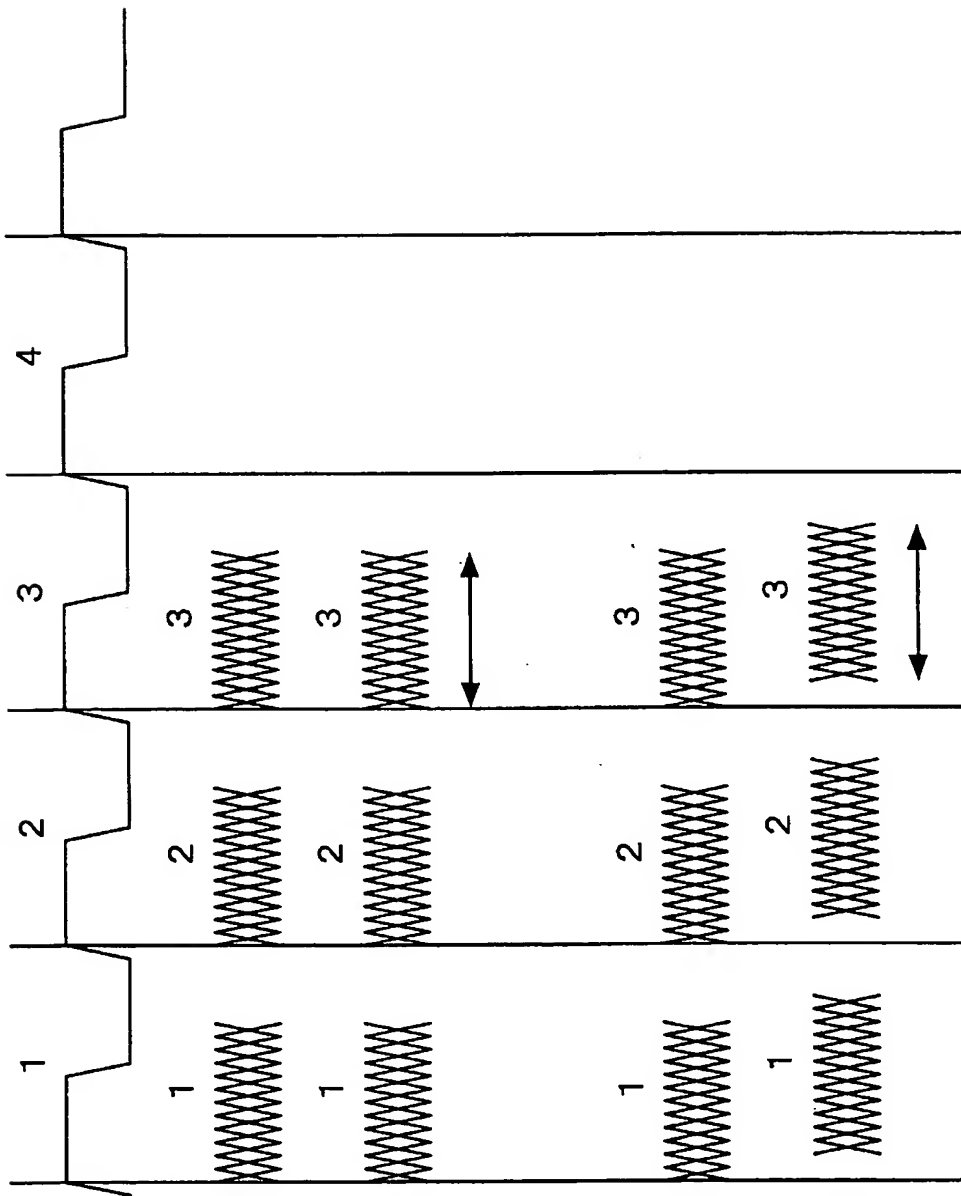


FIG. 5A

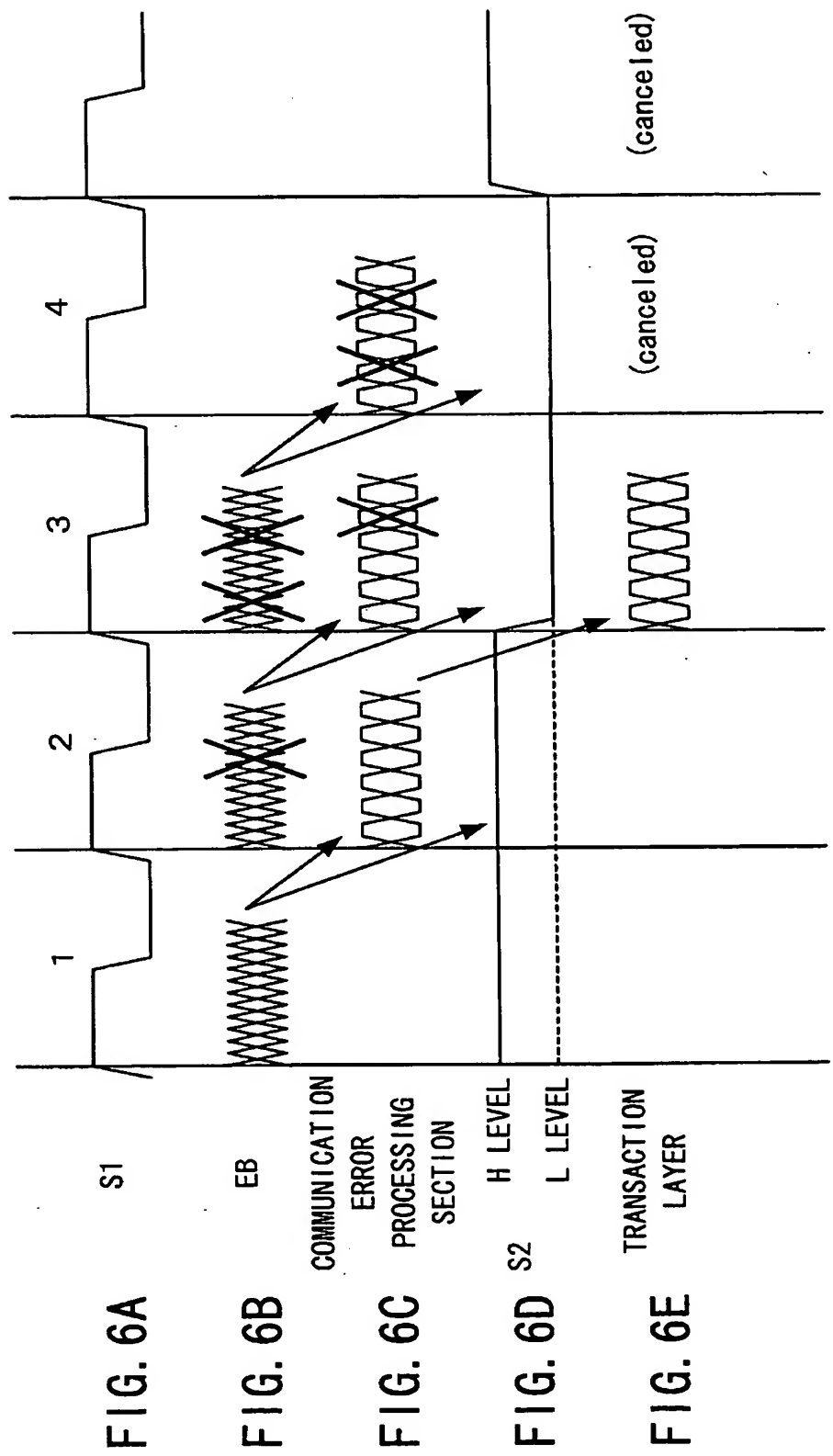
FIG. 5B

FIG. 5C

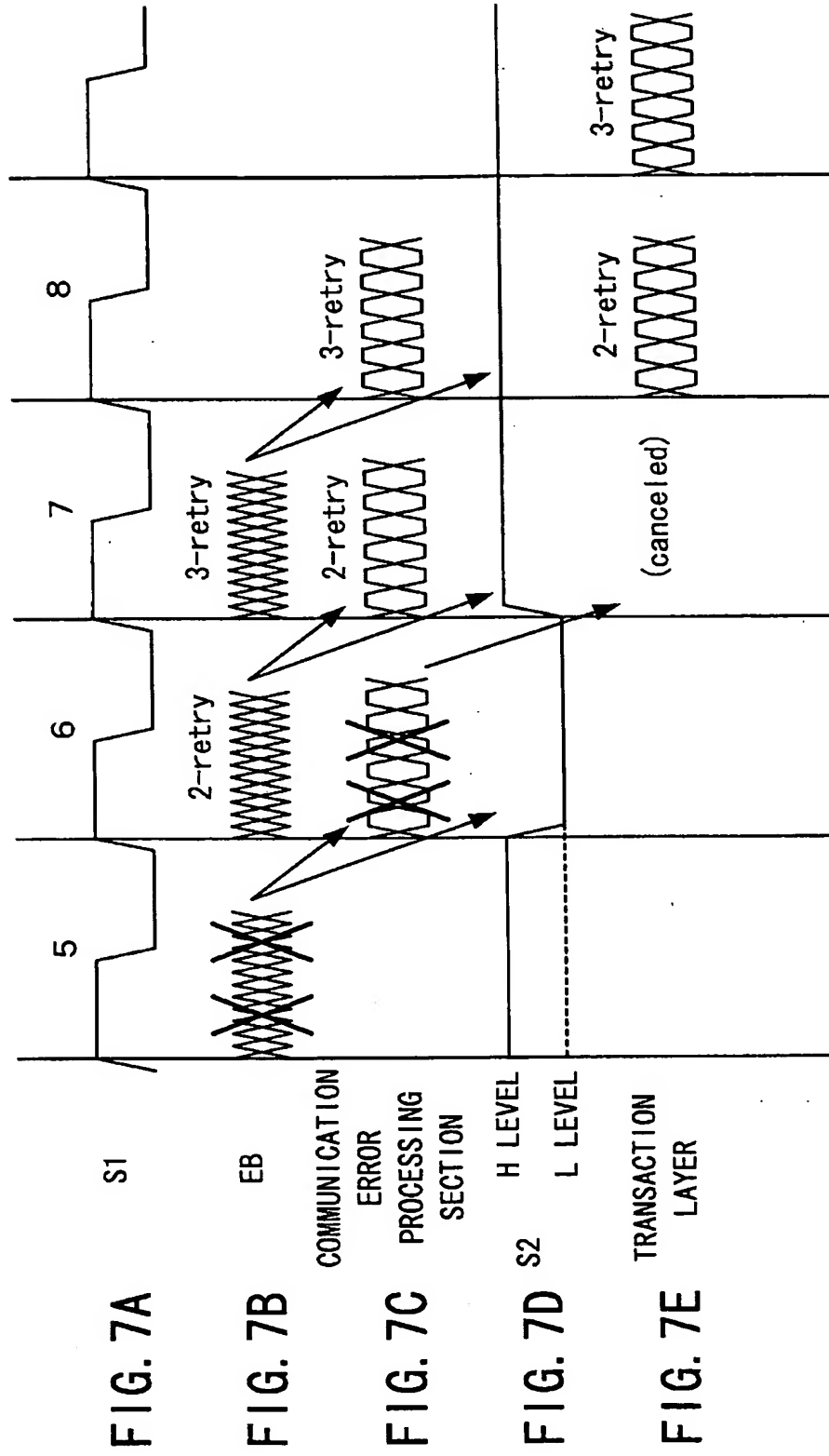
FIG. 5D

FIG. 5E

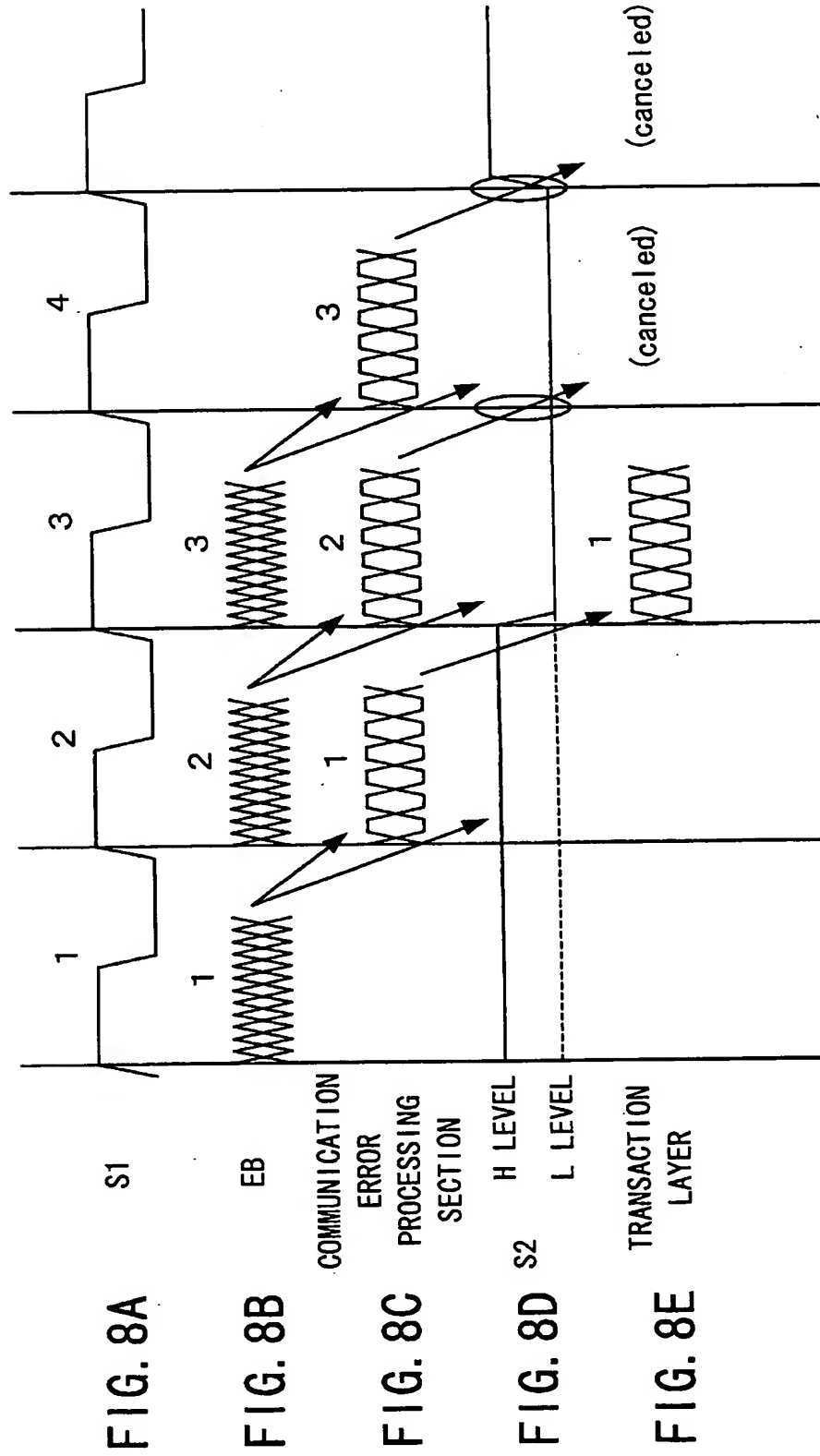
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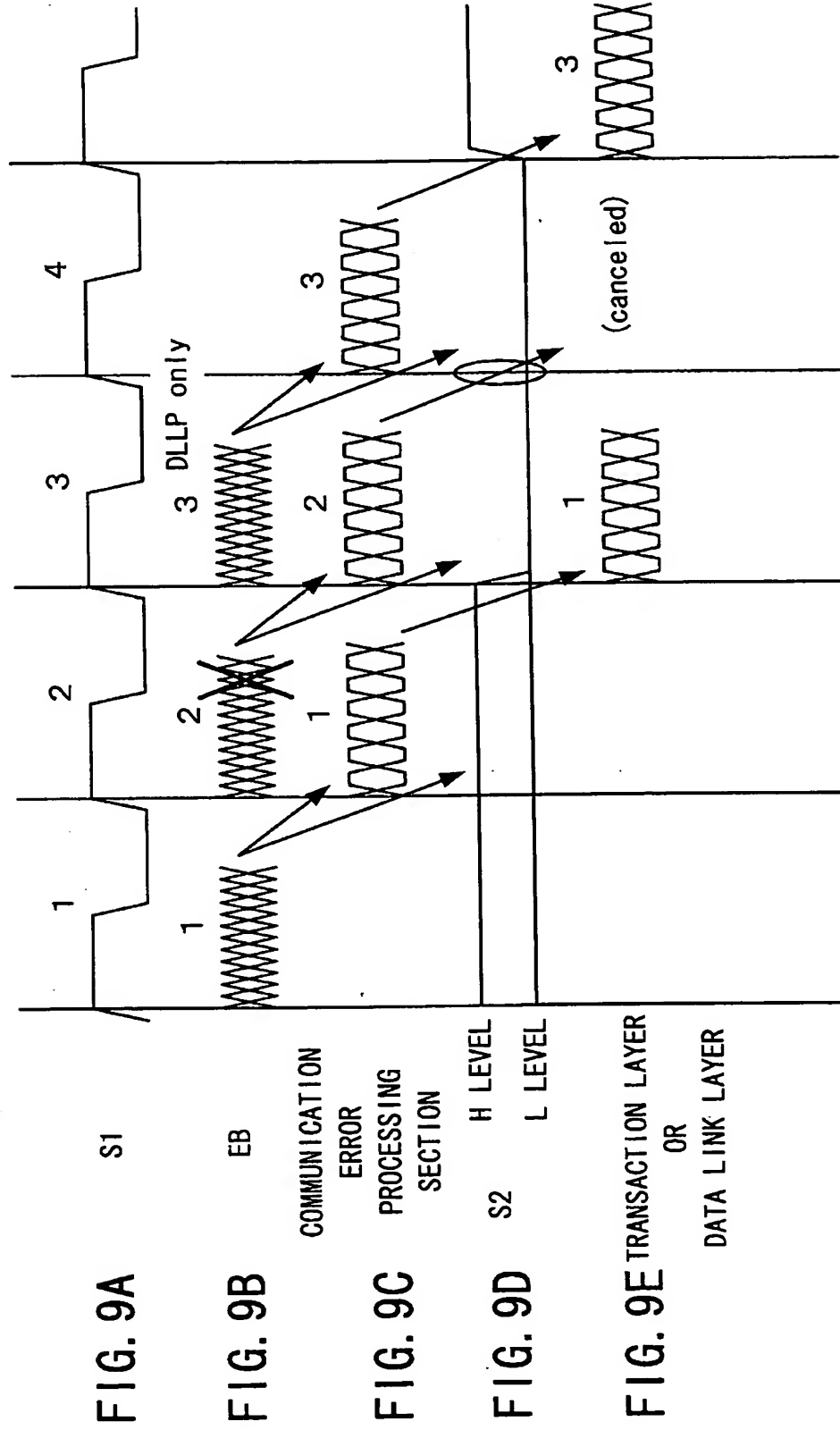


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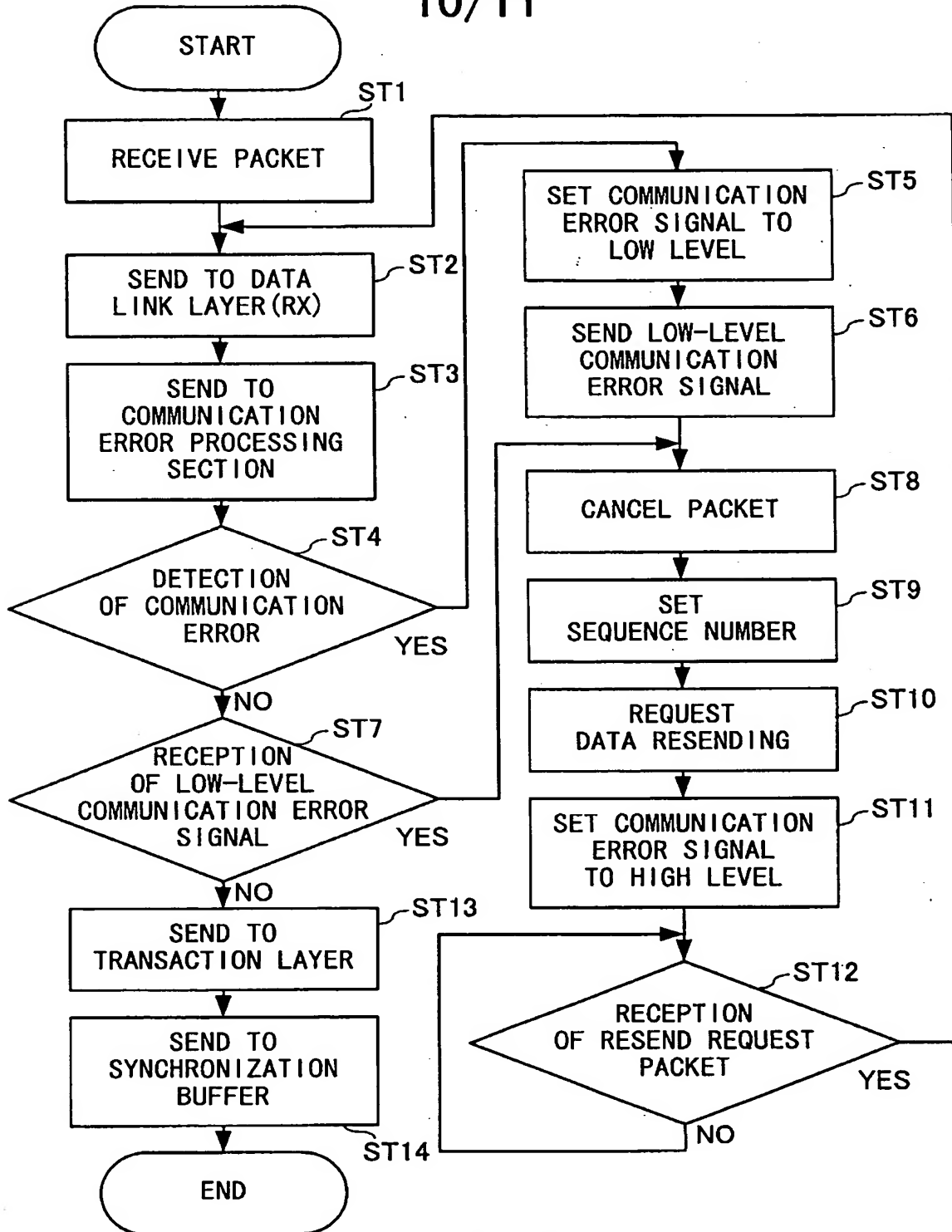


FIG. 10

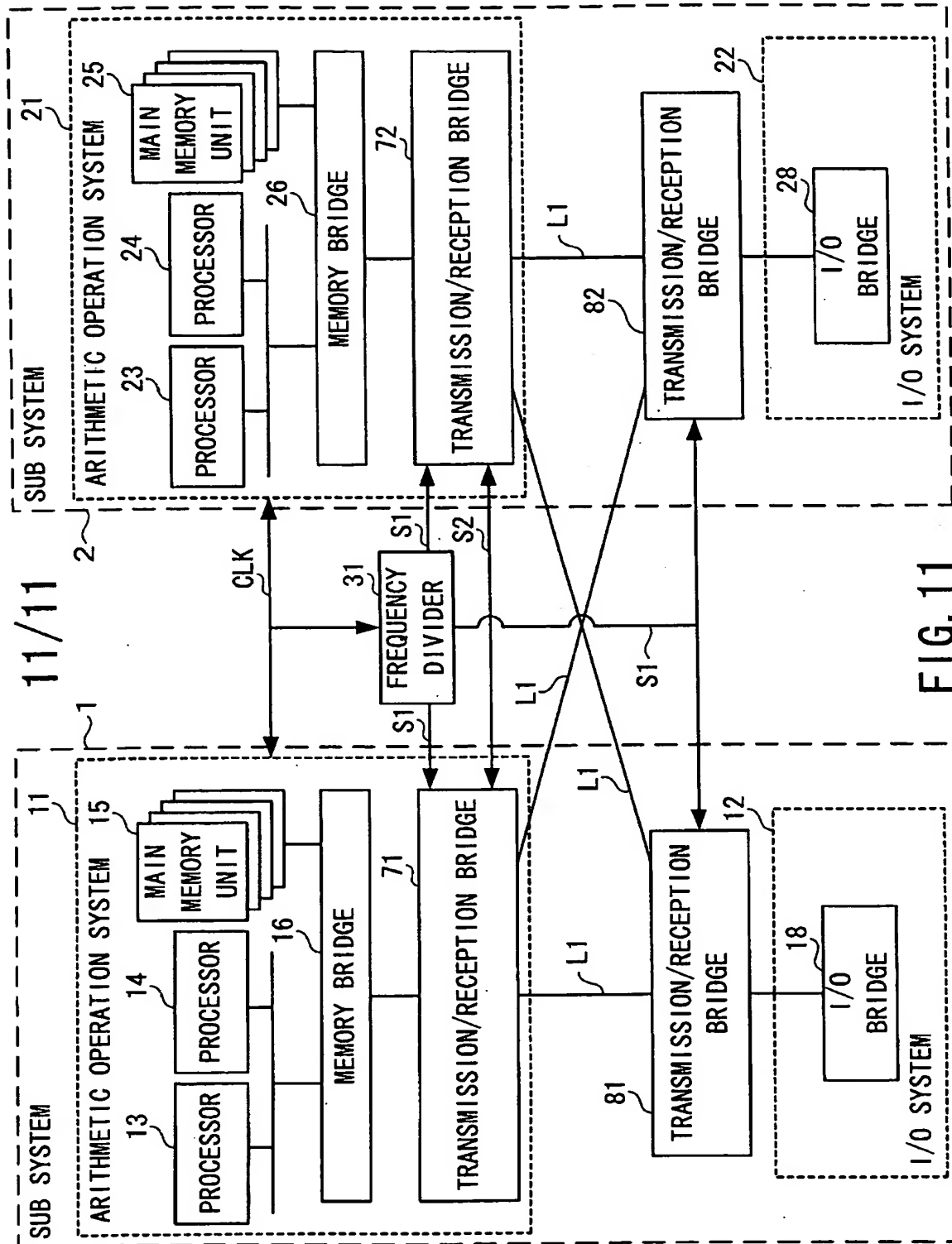


FIG. 11